Abstract

A system and method for accurately detecting an asynchronous frequency within a synchronous digital system. The improved system and method preconditions the asynchronous frequency so that it does not introduce additional phase noise at low frequencies within a digital PLL. The system comprises a digitally controlled oscillator, having a preconditioner and a digital phase locked loop. The preconditioner receives an input clock signal and outputs a modified clock signal that is synchronized to a master clock signal. The digital phase locked loop receives the modified clock signal output from the preconditioner and outputs an output clock signal that is a version of the input clock signal synchronized to the master clock signal. The preconditioner preferably has a higher bandwidth than the digital PLL, and the preconditioner operates to noise shape phase noise of the synchronization to higher frequencies. The digital phase locked loop may then operate to remove the phase noise at the higher frequencies. Due to the operation of the preconditioner, the digital phase locked loop does not introduce phase noise to the synchronized version of the input clock signal.